REMARKS

Claims 1-22 are pending in the application, and are rejected. Claims 1 and 8 are herein amended.

Drawings

The Examiner asserts the Figure 8 should be designated by a legend such as --Prior Art— and asserts that only that which is old is illustrated.

Applicants respectfully disagree with this objection, and note that the specification merely recites on page 3, lines 3 *et seq.*, "the semiconductor film ... which is used here", meaning the semiconductor film as used in the present invention. Applicants respectfully submit that the addition to claim 8 as requested by the Examiner is unnecessary.

However, Applicants note that Fig. 5 is a microphotograph showing a surface state of a section of a transistor manufactured that was subject to a prior art etching process (isotropic) but consists of a semiconductor layer as described in the presently claimed process steps. Therefore, the label "Related Art" is appropriate here. Applicants herewith add the label.

Specification

The Examiner asserts that the title of the invention is not clearly indicative of the invention. Applicants herein change the title to read, "Manufacturing Method of Semiconductor Device Including an Anisotropic Etching Step".

Claim Objections

Claims 1-7 are objected to because the term "another" in line 10 of claim 1 should be changed to "an other". Applicants include this amendment herewith.

Claim Rejections - 35 U.S.C. §112

Claims 1-22 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Applicants respectfully disagree with this rejection. With respect to the Examiner's comment that there is no support in the detailed description of the disclosure for "forming on an entire surface..., and a high content of the other semiconductor element in an intermediate layer region", which are features of claims 1 and 8, Applicants note the following:

On page 3, lines 3-24 of the present specification, it is explained that when isotropic plasma etching is performed for a compound semiconductor film, which has a composition with a high content of Si in its upper layer region and lower layer region, and a high content of the other semiconductor element in an intermediate layer region, the compound semiconductor film after etching is in a state with so-called "voids".

Likewise, on page 10 and page 11, lines 1-16 of the present specification, it is explained that when isotropic plasma etching is performed for an SiGe/SiGeC film, which is a compound semiconductor film cited in the embodiment, the intermediate layer region of the SiGe/SiGeC film is got rod of, and the SiGe/SiGeC film after etching is in the state with "voids". The embodiment as a whole discloses the method for avoiding a compound semiconductor film from being in the state with "voids" in a manufacturing process of a semiconductor device.

It is also disclosed in Fig. 2A and page 8 (lines 23-28) that the SiGe/SiGeC film is grown on an entire surface. Accordingly, Applicants respectfully submit that there is enough support in the embodiment for "forming on an entire surface..., and a high content of the other semiconductor element in an intermediate layer region", which are features of claims 1 and 8.

Additionally, with respect to the Examiner's assertion that an intermediate layer region is formed on the side wall of opening 8, we would like to insist that it is a SiGe/SiGeC film 9 that is formed on the side wall of opening 8, not an intermediate layer region. Besides, with respect to the Examiner's assertion that the side wall of the opening 8 has a high content of silicon, Applicants submit that it is explained in the corresponding part of the embodiment that etching in the lateral direction is not performed in anisotropic dry etching, and a lower layer portion of the SiGe/SiGeC film 9 with high content of Si remains at the side wall of the opening 8.

Claim Rejections - 35 U.S.C. §103

Claims 1-2, 4, 6, 8-9, 11-12, 14, 16-17, 19-20 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Asai et al. (U.S. Patent No. 6,713,790) in view of Applicant's admitted prior art (AAPA).

The Examiner notes that Asai et al. does not teach a compound semiconductor film having upper layer region, a lower layer region, and an intermediate region having the relative contents of the semiconductor elements. The Examiner notes that the present specification teaches in pages 2-3 that it is conventional to obtain a compound semiconductor film which contains silicon and another semiconductor element, and has a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region. The Examiner concludes that it would

have been obvious to use a compound semiconductor film having a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region in the device of Asai et al. in order to simplify the processing steps of making the device by using a conventional processing method.

Applicants respectfully disagree with the Examiner's characterization of the Applicant's admitted prior art. Applicants note that the specification merely recites that if one skilled in the prior art were to assemble a semiconductor film having the claimed parameters, a semiconductor having undesirable voids would be formed. This is strong indication that one skilled in the art at the time of the invention would not have been motivated to combine the steps of providing a semiconductor film having the recited limitations with any etching technique.

The Examiner asserts that claims 1, 8 and 11 do not preclude the compound semiconductor film from being isotropically dry-etched, because the claim uses the transitional phrase "comprising", which does not preclude that which is not recited. Applicants herein amend the claims by adding a limitation to claims 1 and 8 to specifically preclude isotropic etching.

Regarding the remainder of the rejection under §103, Applicants note that Asai et al. discloses anisotropic dry etching for polysilicon films. On the other hand, the invention of claims 1 and 8 (and dependent claims) of the present invention has a feature that a compound semiconductor film is anisotropically dry-etched. When isotropic plasma etching is performed for a compound semiconductor film, the compound semiconductor film following the etching has so-called "voids" and thus is impossible to manufacture a semiconductor device that suits the intended object. The present application focuses on such a problem in the manufacturing process and the problem caused when the isotropic plasma etching are performed for a compound

semiconductor film can be resolved by making a compound semiconductor film anisotropically dry-etched.

Applicants note that Asai et al. does not disclose nor suggest the above-described problem or composition. Accordingly, one skilled in the art at the time of filing of the application would not have been motivated to consider the composition of the present invention on the basis of Asai et al., referring to the compound semiconductor film shown in the Applicant Admitted Prior Art (AAPA), without being aware of the above-described problem.

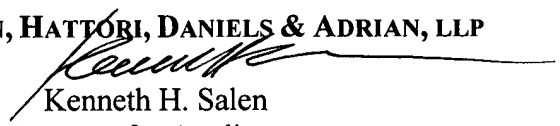
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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Attachments Corrected Fig. 5